Parallel Capacitors and the effect of Antiresonance

Summary

When placing two capacitors in parallel for the purpose of improving decoupling, and those capacitors have different characteristics, the performance of the pair may be worse than that of either type of capacitor on its own —due to the effect of antiresonance.

Introduction

Decoupling capacitors near the power pin(s) of logic ICs are required —there is no disagreement on that. The transitions from low to high, and vice versa, in these ICs cause pulse transients in the supply current of the IC. These transients generate high frequency noise, and without a capacitor near the power pin to filter it out, this noise runs through the power traces all the way to the voltage regulator. Noise on the power line may cause a number of issues, among which conducted or radiated emission (EMC).

Neither is there disagreement on the effects of resonance and antiresonance, in the application of decoupling capacitors. An “ideal” capacitor only has capacitance, but real-world capacitors also have parasitic inductance & resistance (ESL and ESR respectively). The trace to the capacitor likewise contributes some inductance and resistance. A real-world capacitor should therefore be modelled as an RLC filter: it has a resonant frequency, above which the effectiveness of the capacitance is cancelled out by the parasitic inductance.

Where there is disagreement, however, is what conclusions must be drawn from this analysis. For instance, [Archambeault 2002] recommends to always place two capacitors in parallel: one of 100nF and one of 100pF, in order to break the resonance. Contrariwise, [Danker 2011] insists that decoupling recommends *against* placing decoupling capacitors in parallel (regardless of their values). Finally, [Ott 2009] recommends putting two capacitors in parallel, but in contrast to Archambeault he asserts that both should be identical,[1] citing the risk of antiresonance.

1 The reason for still recommending two capacitors in parallel, even though both are identical, is that this halves the ESL and ESR —and lower ESL is always a good thing.

The argumentation for both sides in this debate has a weak spot —at least in my view. The PCB layout that [Archambeault 2002] used for his experiment, almost guarantees resonance all over the board, but it is an unrealistic design. His conclusions therefore cannot be mapped to real-world PCB designs. [Ott 2009] *simulated* the antiresonance and its magnitude, rather than measuring it —but doubt on the validity of a simulation remains, until it is validated.

Therefore, the objective of this white paper is to present well-documented measurements, focussed on the core matter of contention: is it beneficial or harmful to place capacitors with different values in parallel?

Frame of reference

The ESL value is rarely documented in data sheets. For ballpark measures, the values for a few general purpose ceramic capacitors are in the table below (information taken from Kemet).

part number	value	size	F_{res} (MHz)	ESL (nH)
C0402C104J4RAC	100nF	0402	29.4	0.26
C0603C104K4PAC	100nF	0603	19.5	0.67
C0805C104K6RAC	100nF	0805	20.3	0.62
C1206C104K6RAC	100nF	1206	17.7	0.80
C0402C101K1TAC	100pF	0402	524	0.92
C0603C101K4RAC	100pF	0603	915	0.30
C0805C101K4RAC	100pF	0805	692	0.53

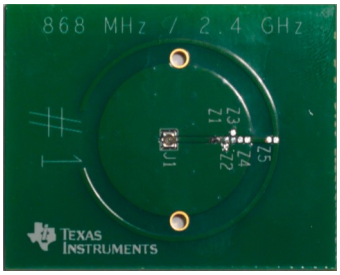
Note that the *effective* ESL is dependent on the full current loop —so, including traces and vias leading up the capacitor. See also [Cain 2020] for values measured on a few AVX ceramic capacitors.

For completeness, the relation between the capacitance, (parasitic) inductance and the resonant frequency is:

$$F_{res} = \frac{1}{2\pi\sqrt{L \cdot C}}$$

Experiment set-up

For the base PCB, we used board #1 from the Texas Instruments “antenna development kit” (product number CC-ANTENNA-DK2). This is a kit for evaluating various antenna designs, but we used it with the antenna *disconnected* and replaced by a second RF-connector.



The rationale is that the board has an RF-connector, for easy connection to a VNA (vector network analyser), a short trace designed to have an impedance of 50Ω, and a set of footprints on that trace for mounting the various configurations of (parallel) capacitors.

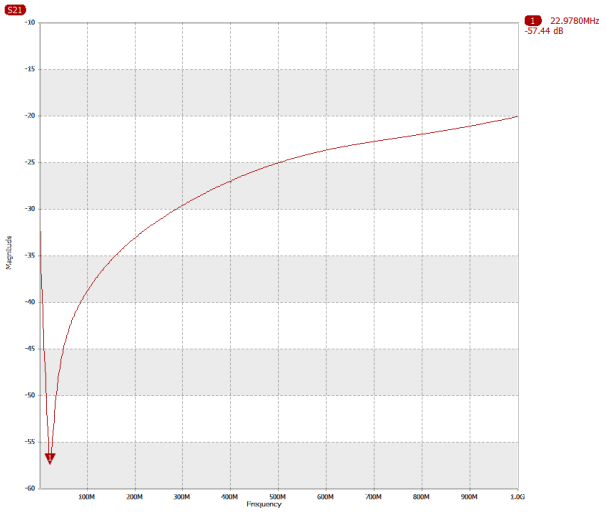
For the test, we selected MLCC capacitors with values of 100pF and 100nF, in conformance to the recommendations in [Archambeault 2002]. The capacitors used in the tests are:

part number	value	attributes
C0402C101J2GACAUTO	100pF	C0G
C0402C104J4RAC	100nF	X7R
C0402C103J4RAC	10nF	X7R

We used a VNA to plot the S21 magnitude of the capacitor configurations were tested with a VNA, in the range 1MHz to 1GHz. Note that in the graphs, the frequency scale is linear (rather than logarithmic).

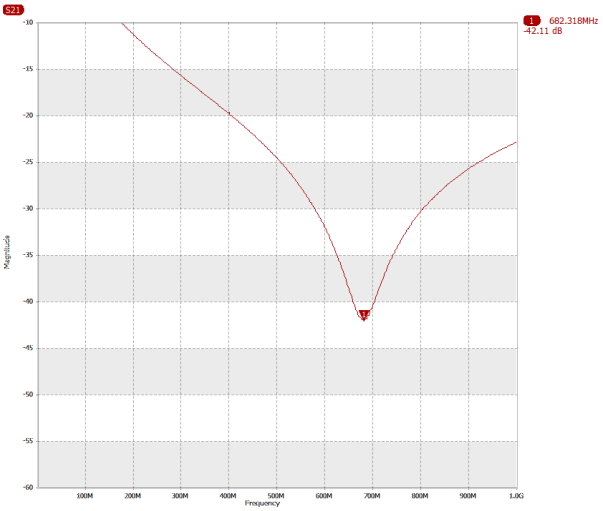
Results

[1] Single 100nF capacitor



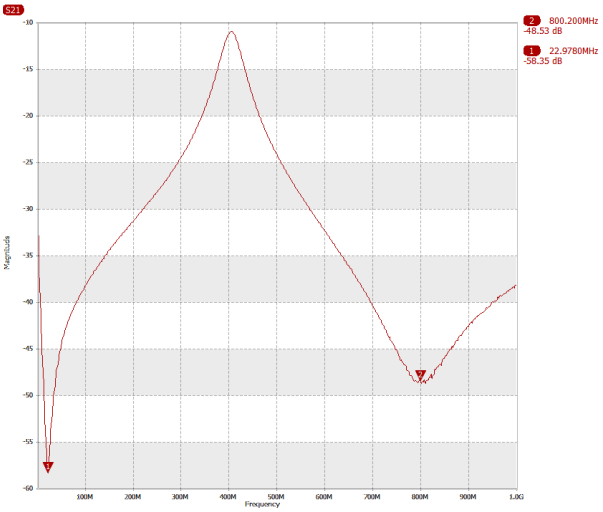
Single 100nF capacitor, resonant at (roughly) 21MHz. The disparity of this measured value and the resonant frequency of this capacitor according to the manufacturer (Kemet, 29.4MHz, see the table on page 1), is likely due to trace inductance of the test board —as said, the effective ESL depends on the full current loop.

[2] Single 100pF capacitor



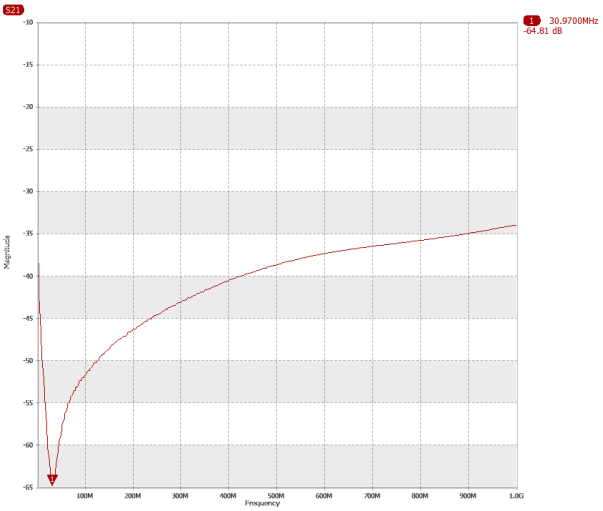
Single 100pF capacitor, resonant at 682MHz.

[3] 100nF and 100pF capacitors in parallel



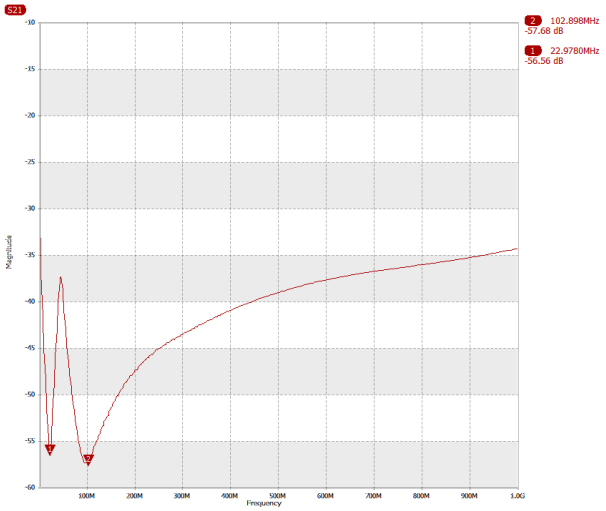
Two resonant frequencies, with a peak halfway clearly demonstrating antiresonance.

[4] Two 100nF capacitors in parallel



Note the different scale on this graph (to make the graph fit). Also note the changed resonant frequency of the pair, compared to the resonant frequency of a single 100nF capacitor (nearly 31MHz versus nearly 21MHz).

[5] 100nF and 10nF capacitors in parallel



Since the properties of a 100nF capacitor and of a 100pF capacitor are quite far apart, we also did a test with a pair that was closer to each other.

Analysis

The measurements demonstrate the effect of antiresonance when two capacitors with different characteristics are mounted in parallel.

However, keep in mind that antiresonance does not *generate* noise at that frequency; it is simply (significantly) less effective at *suppressing* it. The choice of decoupling strategy therefore depends on which parasitic frequencies are actually present.

Another note is that on a real-world PCB, there will typically be multiple ICs, each of which need decoupling. These capacitors are in parallel. Regardless of whether all these decoupling capacitors are the same or different, their *effective* ESL may be different —because of different trace lengths, and possibly vias. Hence, antiresonance is not simply ruled out by using a single capacitor type for all decoupling capacitors.

As a rule-of-thumb, though, mounting multiple capacitors of the same type in parallel will generally improve decoupling (compare test [4] with test [1]), whereas mixing capacitor types for decoupling may well be counter-productive. Observe, for example, how test [5] improves on test [4] only in the area around 100MHz, while it performs significantly worse around 50MHz.

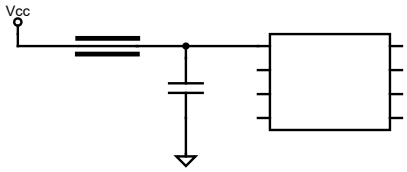
Alternative options

The goal of mounting capacitors in parallel is to reduce ESL and ESR, and thereby be more effective in filtering out high-frequency noise. However, it is not the only solution.

An obvious alternative is to use a single low-ESL capacitor instead of the pair of parallel capacitors. The *flip-type* (or “reverse geometry”) package for capacitors, with wide pads and a narrow body, was designed with exactly the goal of reducing ESL. So instead of a capacitor in the common 0603 package (1.6 mm long, 0.8 mm wide), you can opt for a capacitor in 0306 package (0.8 mm long, 1.6 mm wide): it takes the same space on the PCB, has the same essential specifications (regarding capacitance, voltage, tolerance), but with an ESL in the order of 0.14 nH (compared to 0.30 nH for the 0603 package).

Feed-through capacitors also reduce ESL, by annulling lead/trace inductance and lowering ground inductance. Feed-through capacitors are designed for filtering high frequencies out of power or data lines.

Another option is to place a ferrite bead in the power line, before the decoupling capacitor (see below). This is a two-component solution (like parallel capacitors), so there is no gain in board space or placement cost.



References

Archambeault, Bruce R.; *PCB Design for Real-World EMI Control*; Springer; 2002.

Cain, Jeffrey; *Parasitic Inductance of Multilayer Ceramic Capacitors*; AVX Corporation; 2020.

Danker, Berend; *Fundamentals of Electromagnetic Compatibility*; second edition; Bicon Laboratories; 2011.

Ott, Henry W.; *Electromagnetic Compatibility Engineering*; Wiley; 2009; ISBN 978-0470189306.

Togashi, Masaaki; *Low-ESL Multilayer Ceramic Capacitors*; TDK Corporation; 2011.

Colophon

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